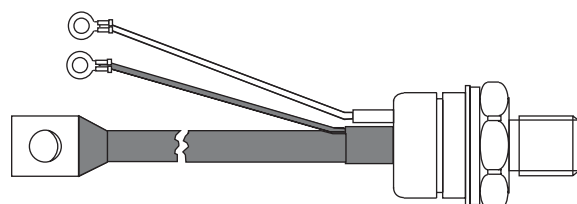


Inverter Grade Thyristors (Stud Version), 175 A



TO-209AB (TO-93)

FEATURES

- All diffused design
- Center amplifying gate
- Guaranteed high dV/dt
- Guaranteed high dI/dt
- High surge current capability
- Low thermal impedance
- High speed performance
- Compression bonding
- Lead (Pb)-free
- Designed and qualified for industrial level



RoHS
COMPLIANT

PRODUCT SUMMARY

$I_{T(AV)}$	175 A
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TYPICAL APPLICATIONS

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

MAJOR RATINGS AND CHARACTERISTICS

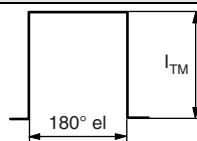
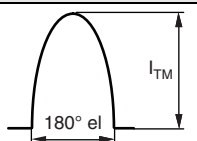
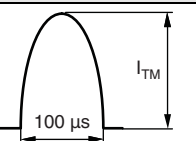
PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		175	A
	T_C	85	°C
$I_{T(RMS)}$		275	A
I_{TSM}	50 Hz	4680	
	60 Hz	4900	
I^2t	50 Hz	110	kA ² s
	60 Hz	100	
V_{DRM}/V_{RRM}		1000 to 1200	V
t_q	Range	15 to 25	μs
T_J		- 40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	VOLTAGE CODE	V_{DRM}/V_{RRM} , MAXIMUM REPETITIVE PEAK VOLTAGE V	V_{RSM} , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	I_{DRM}/I_{RRM} MAXIMUM AT $T_J = T_J$ MAXIMUM mA
ST173S	10	1000	1100	40
	12	1200	1300	

CURRENT CARRYING CAPABILITY

FREQUENCY							UNITS
50 Hz	500	320	790	550	4510	3310	A
400 Hz	450	290	810	540	1970	1350	
1000 Hz	330	190	760	490	1050	680	
2500 Hz	170	80	510	300	480	280	
Recovery voltage V_r	50		50		50		V
Voltage before turn-on V_d	V_{DRM}		V_{DRM}		V_{DRM}		
Rise of on-state current di/dt	50		-		-		A/ μ s
Case temperature	60	85	60	85	60	85	°C
Equivalent values for RC circuit	47/0.22		47/0.22		47/0.22		Ω/μ F

ON-STATE CONDUCTION

PARAMETER	SYMBOL	TEST CONDITIONS			VALUES	UNITS
Maximum average on-state current at case temperature	I _{T(AV)}	180° conduction, half sine wave			175	A
					85	°C
Maximum RMS on-state current	I _{T(RMS)}	DC at 75 °C case temperature			275	A
Maximum peak, one half cycle, non-repetitive surge current	I _{TSM}	t = 10 ms	No voltage reapplid	Sinusoidal half wave, initial T _J = T _J maximum	4680	
		t = 8.3 ms			4900	
		t = 10 ms	100 % V _{RRM} reapplid		3940	
		t = 8.3 ms			4120	
Maximum I ² t for fusing	I ² t	t = 10 ms	No voltage reapplid		110	kA ² s
		t = 8.3 ms			100	
		t = 10 ms	100 % V _{RRM} reapplid		77	
		t = 8.3 ms			71	
Maximum I ² √t for fusing	I ² √t	t = 0.1 to 10 ms, no voltage reapplid			1100	kA ² √s
Maximum peak on-state voltage	V _{TM}	I _{TM} = 600 A, T _J = T _J maximum, t _p = 10 ms sine wave pulse			2.07	V
Low level value of threshold voltage	V _{T(TO)1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			1.55	
High level value of threshold voltage	V _{T(TO)2}	I > π × I _{T(AV)} , T _J = T _J maximum			1.58	
Low level value of forward slope resistance	r _{t1}	(16.7 % × π × I _{T(AV)}) < I < π × I _{T(AV)} , T _J = T _J maximum			0.87	mΩ
High level value of forward slope resistance	r _{t2}	I > π × I _{T(AV)} , T _J = T _J maximum			0.82	
Maximum holding current	I _H	T _J = 25 °C, I _T > 30 A			600	mA
Typical latching current	I _L	T _J = 25 °C, V _A = 12 V, R _a = 6 Ω, I _G = 1 A			1000	

SWITCHING

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum non-repetitive rate of rise of turned on current	di/dt	$T_J = T_J$ maximum, $V_{DRM} = \text{Rated } V_{DRM}$ $I_{TM} = 2 \times di/dt$	1000	A/μs
Typical delay time	t_d	$T_J = 25$ °C, $V_{DM} = \text{Rated } V_{DRM}$, $I_{TM} = 50$ A DC, $t_p = 1$ μs Resistive load, gate pulse: 10 V, 5 Ω source	1.1	μs
Maximum turn-off time	minimum	$T_J = T_J$ maximum, $I_{TM} = 300$ A, commutating $di/dt = 20$ A/μs $V_R = 50$ V, $t_p = 500$ μs, dV/dt : See table in device code	15	
	maximum		25	



BLOCKING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 80 % V_{DRM} , higher value available on request	500	V/ μ s
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM}	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	40	mA

TRIGGERING				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $f = 50$ Hz, $d\% = 50$	60	W
Maximum average gate power	$P_{G(AV)}$		10	
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms	10	A
Maximum peak positive gate voltage	+ V_{GM}		20	V
Maximum peak negative gate voltage	- V_{GM}		5	
Maximum DC gate current required to trigger	I_{GT}	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω	200	mA
Maximum DC gate voltage required to trigger	V_{GT}		3	V
Maximum DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied	20	mA
Maximum DC gate voltage not to trigger	V_{GD}		0.25	V

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		- 40 to 125	°C
Maximum storage temperature range	T_{Stg}		- 40 to 150	
Maximum thermal resistance, junction to case	R_{thJC}	DC operation	0.105	K/W
Maximum thermal resistance, case to heatsink	R_{thCS}	Mounting surface, smooth, flat and greased	0.04	
Mounting torque, ± 10 %		Non-lubricated threads	31 (275)	N · m (lbf · in)
		Lubricated threads	24.5 (210)	
Approximate weight			280	g
Case style		See dimensions - link at the end of datasheet	TO-209AB (TO-93)	

ΔR_{thJC} CONDUCTION				
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION	RECTANGULAR CONDUCTION	TEST CONDITIONS	UNITS
180°	0.016	0.012	$T_J = T_J$ maximum	K/W
120°	0.019	0.020		
90°	0.025	0.027		
60°	0.036	0.037		
30°	0.060	0.060		

Note

- The table above shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

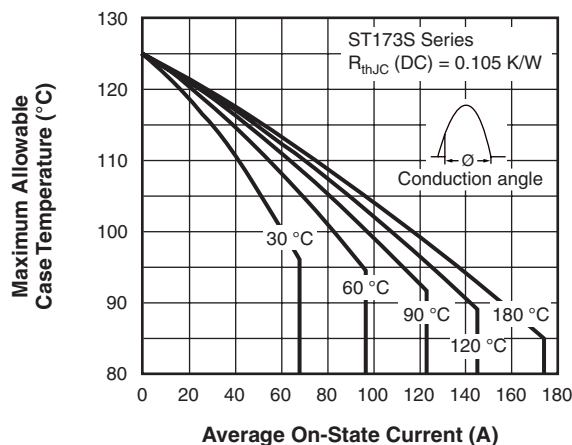


Fig. 1 - Current Ratings Characteristics

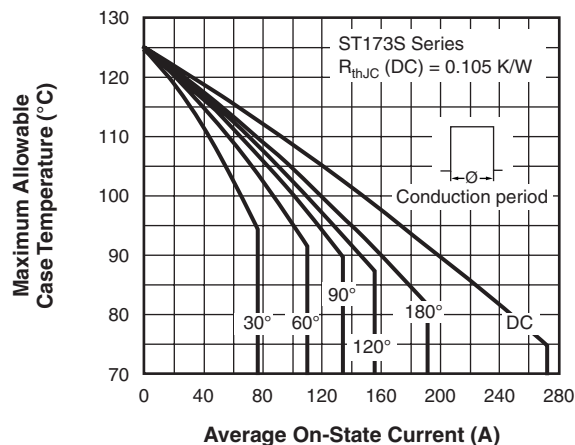


Fig. 2 - Current Ratings Characteristics

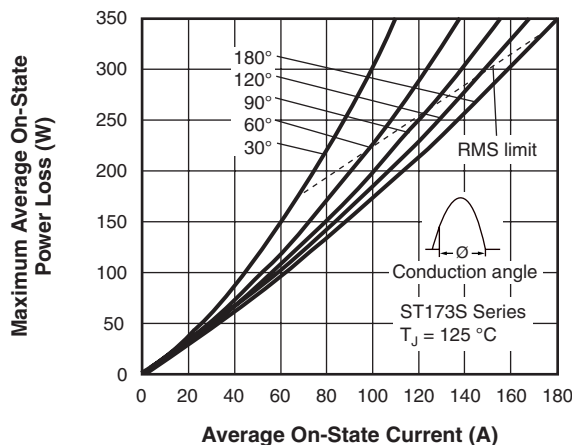


Fig. 3 - On-State Power Loss Characteristics

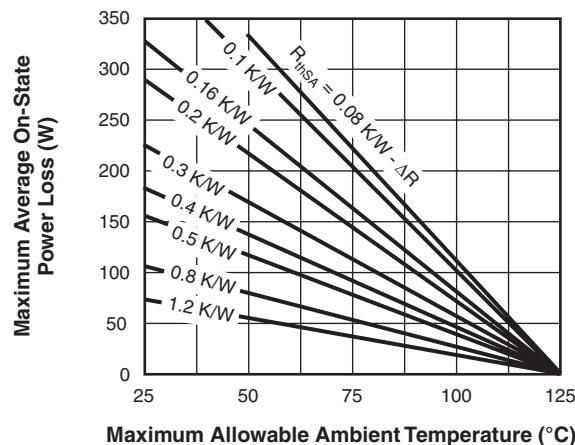


Fig. 4 - On-State Power Loss Characteristics

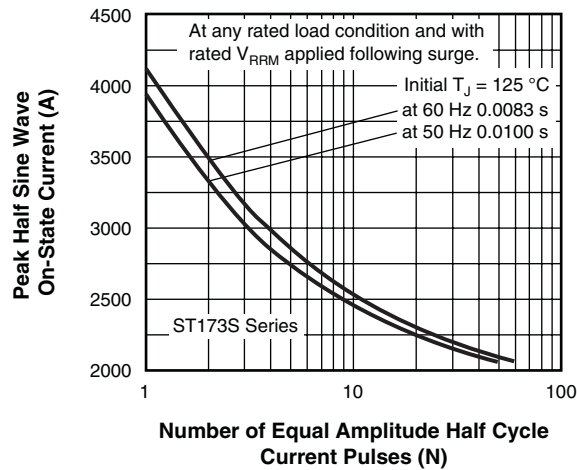


Fig. 5 - Maximum Non-Repetitive Surge Current

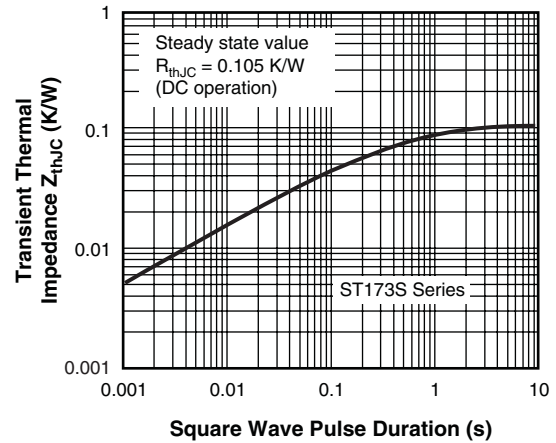


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

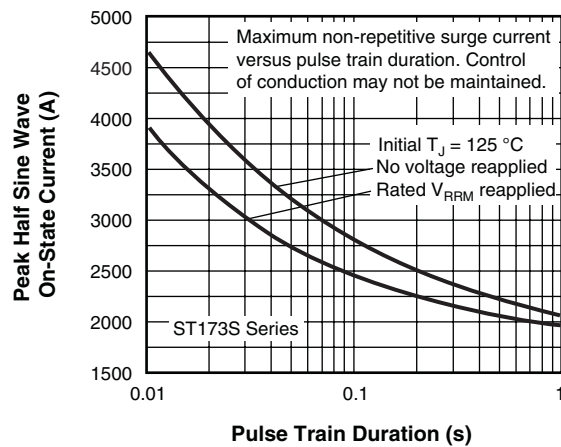


Fig. 6 - Maximum Non-Repetitive Surge Current

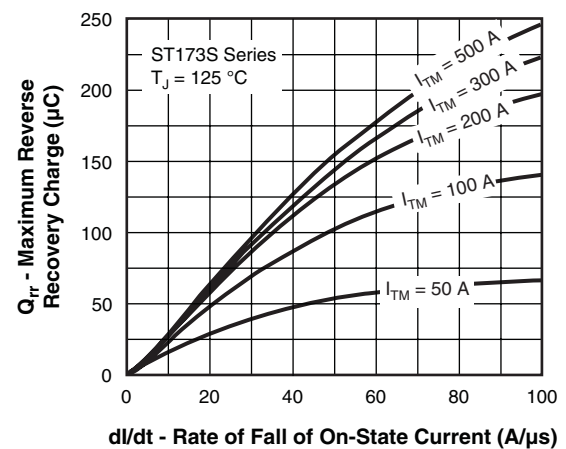


Fig. 9 - Reverse Recovered Current Characteristics

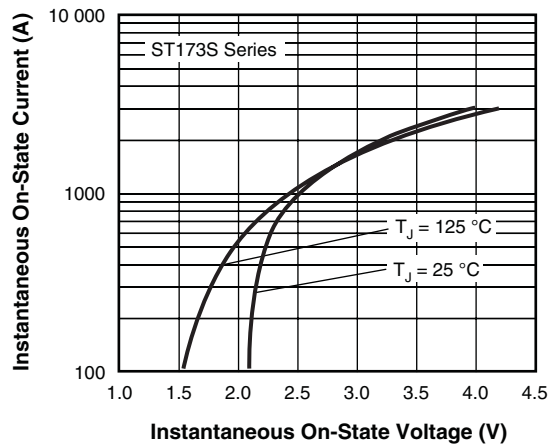


Fig. 7 - On-State Voltage Drop Characteristics

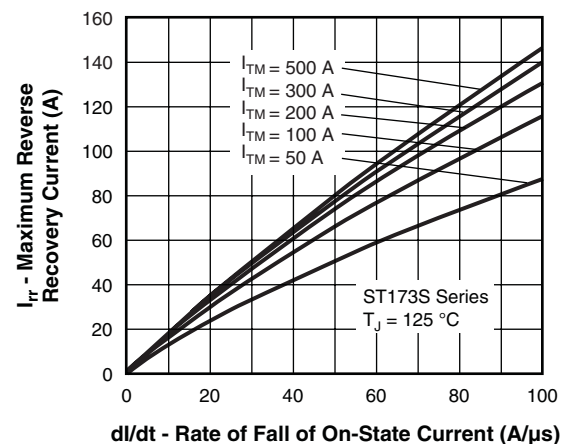


Fig. 10 - Reverse Recovery Current Characteristics

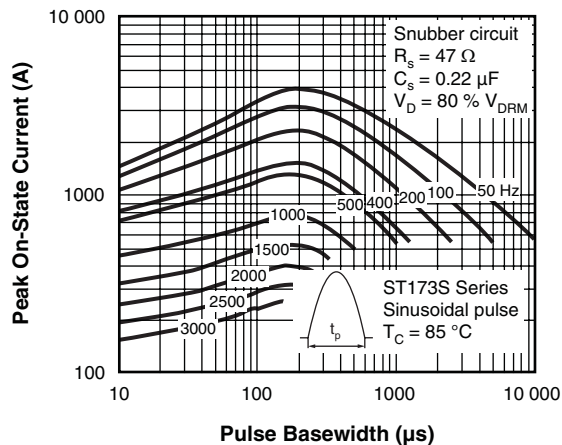
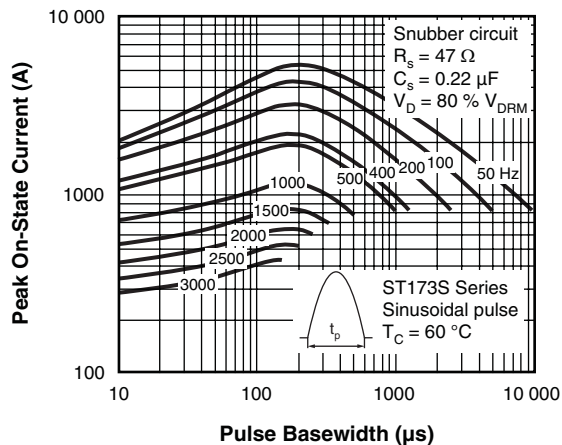


Fig. 11 - Frequency Characteristics

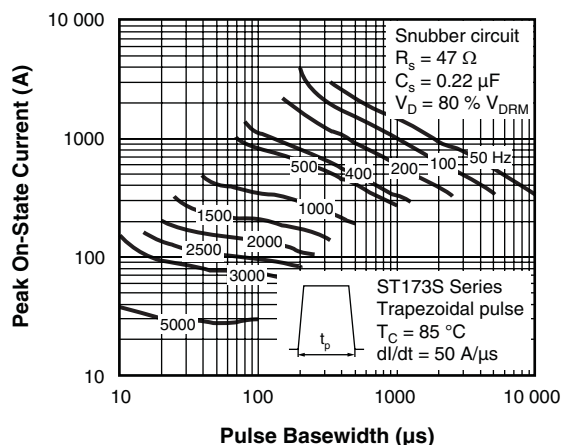
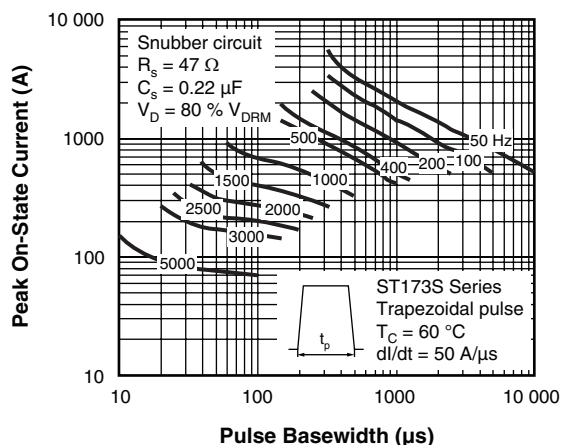


Fig. 12 - Frequency Characteristics

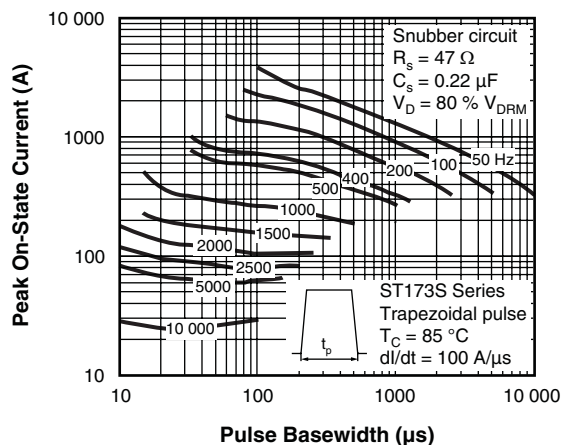
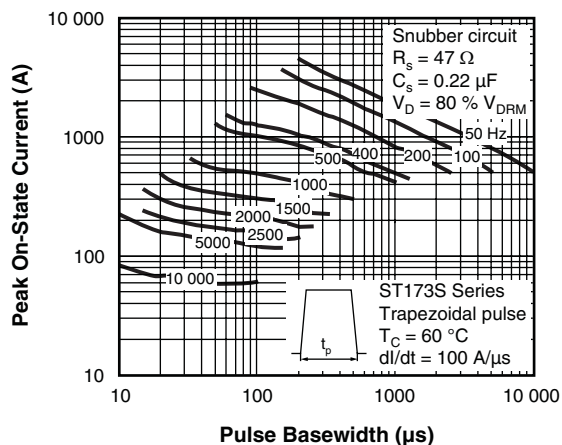


Fig. 13 - Frequency Characteristics

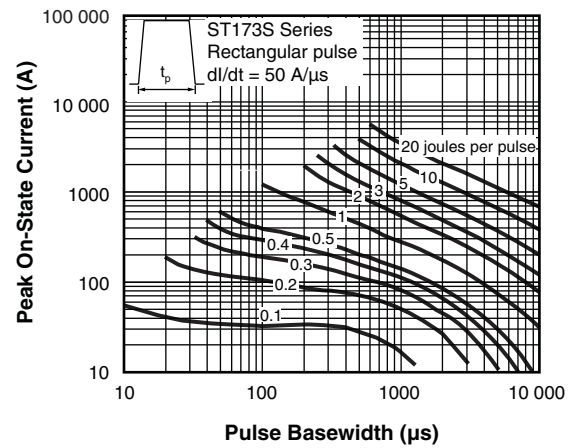
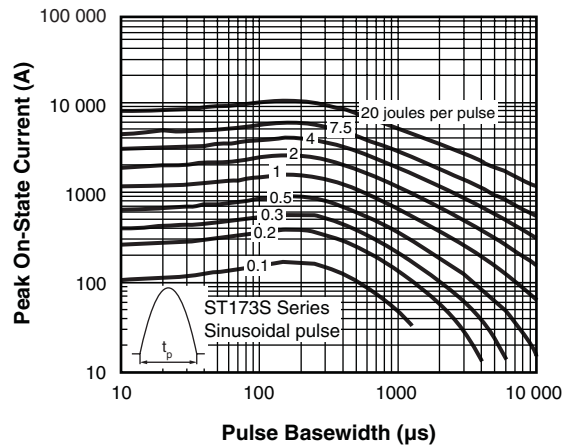


Fig. 14 - Maximum On-State Energy Power Loss Characteristics

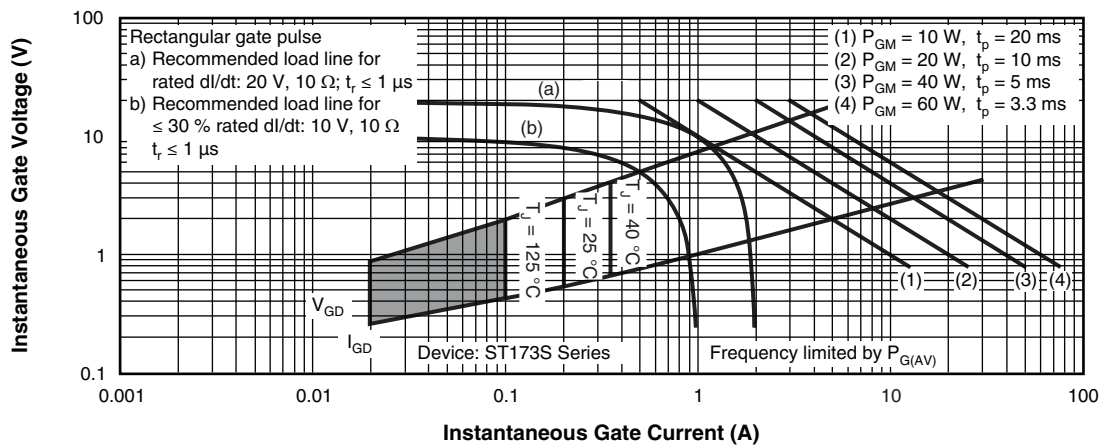


Fig. 15 - Gate Characteristics

ST173SPbF Series

Vishay High Power Products Inverter Grade Thyristors
(Stud Version), 175 A



ORDERING INFORMATION TABLE

Device code	ST	17	3	S	12	P	F	K	0	-	PbF
	1	2	3	4	5	6	7	8	9	10	11

- 1** - Thyristor
- 2** - Essential part number
- 3** - 3 = Fast turn-off
- 4** - S = Compression bonding stud
- 5** - Voltage code x 100 = V_{RRM} (see Voltage Ratings table)
- 6** - P = Stud base 3/4" 16UNF-2A
M = Stud base metric threads M16 x 1.5
- 7** - Reapplied dV/dt code (for t_q test condition)
- 8** - t_q code
- 9** - 0 = Eyelet terminals
(gate and aux. cathode leads)
1 = Fast-on terminals
(gate and aux. cathode leads)
2 = Flag terminals (for cathode and gate terminals)
- 10** - Critical dV/dt:
 - None = 500 V/ μ s (standard value)
 - L = 1000 V/ μ s (special selection)
- 11** - Lead (Pb)-free

dV/dt - t_q combinations available					
dV/dt (V/ μ s)	20	50	100	200	400
15	CL	-	-	-	-
18	CP	DP	EP	FP*	-
20	CK	DK	EK	FK*	HK
25	CJ	DJ	EJ	FJ	HJ
30	-	DH	EH	FH	HH

* Standard part number.
All other types available only on request.

LINKS TO RELATED DOCUMENTS	
Dimensions	http://www.vishay.com/doc?95079



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